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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/751,714
Filing Date: January 05, 2004
Appellant(s): LUK ET AL.

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For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/9/09 appealing from the Office action mailed.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,386,151	FOLMSBEE	1-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The ground(s) of rejection set forth in the appealed Final Office action mailed 8/22/09 is herewith reproduced for the appealed claims 24-25 (only).

BEGINNING OF THE GROUNDS OF REJECTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 24-28, 36 and 37*** are rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee (5,386,151).

Folmsbee teaches as prior art (Figure 1A and col. 4, l. 1-65) a method for amplifying signals ("Description of the Preferred Embodiment", col. 1, l. 29-32 and col. 3, l. 57-67), the method comprising:

determining that a voltage on a signal line (signal line from VDD, as arriving at node 125) is to be amplified;

modifying voltage on a control line ϕ' (providing clock input ϕ' under gate of MOS capacitor 130) (col. 4, l. 1-33), wherein the control line is coupled to a second terminal (source-drain terminal) of a two-terminal semiconductor device (MOS capacitor 130) (Fig. 1A and loc.cit.), the two-terminal device having said second terminal and a first terminal (gate), the first terminal coupled to the signal

line (Fig. 1A and loc.cit.) , the second terminal coupled to the control line (see above), wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is in a first voltage range and to have a lower capacitance when a voltage on the first terminal (gate) is in a second voltage range (inherently so because the MOS capacitor's conductive channel width and conductivity depends thus on gate voltage), wherein said first and second voltage ranges are defined by a threshold voltage (inherently so, for the formation of a conductive channel is characterized by a threshold voltage), and wherein the control line is adapted to be coupled to a control signal (clock signal ϕ') and wherein the signal line is adapted to be coupled to a signal and to be an output VOUT of the circuit (through 140); and

wherein an isolation device (NMOS transistor 110) is intermediate the signal line and the two-terminal semiconductor device, the isolation device having an input, an output and a control terminal (gate of NMOS transistor 110), the input of the isolation device coupled to the signal line (at node 125) and the output of the isolation device coupled to the first terminal 130 (through node 135), wherein the output of the isolation device is adapted to be output of "the" circuit, interpreted to be "output of the amplifier", and wherein the method further comprises the step of applying a control voltage to the control terminal of the isolation device (a gate voltage is inherently applied to the NMOS transistor's gate when is use), the control voltage being greater than a threshold voltage of

the isolation device (as otherwise the isolation device would be a perfect and permanent insulator while no voltage would be communicated).

On claim 25: the limitation is met because the "expected" voltage for a signal coupled to the input of the isolation device is the voltage at node 125, which is added to the voltage on the gate of NMOS transistor 110, i.e., the isolation device (see col. 4, l. 34-40), the gate thereof being in series with said node 125, and the clock input ϕ in a high state adding to the pre-charge voltage at 125 the clock swing of clock input ϕ.

(10) Response to Argument

10.1: Appellant's first Argument (page 4, lines 22-24):

Appellant alleges: "There is NO disclosure in Folmsbee to *determine* that a voltage on a signal line is to be amplified and the Examiner has not cited any teaching in Folmsbee that discloses this limitation" (see page 4 of Appeal).

Examiner disagrees for the following reason: Folmsbee discloses as Prior Art a charge pump circuit, which is for voltage amplification and which is actually used to increase the amplitude of a voltage communicated to node 125 of the circuit. Examiner pointed to the arrival of the voltage at node 125 that is subsequently amplified. Said arrival clearly is the first step of the amplification process and hence shows the determination of the user to subject the voltage to the amplification process. In other words: the user must have determined that said voltage needed amplification, because otherwise the voltage would not have been imposed on node 125 since amplification is the very purpose of the charge pump. Furthermore, for disclosure appellant refers to Figure 13 and related text in the specification including voltage waveforms obtained by

the amplifier of Figure 13, i.e., Figure 14 and discussion (page 20, line 26 – page 21, line 21) on a possible operation of the gate diode sense amplifier 1300 of Figure 13, while said discussion only discloses two case distinctions: a small voltage and a zero voltage, where clearly only the former is to be amplified. Therefore, within the context of the amplifier 1300 to which appellant refers a small voltage arrives at a node and is consequently amplified, in analogy with the arrival of a voltage VDD-VT at node 125 and its consequent amplification. Finally, examiner notes that “determined” on page 21 (line 13) apparently only has the meaning of "resulted".

10.2: Appellant’s second Argument (page 4, lines 25-29):

Appellant alleges: “appellants note that a signal line carries information”, while: “The line from VDD to node 125 does not carry information”.

Examiner disagrees for the following reason:

“The voltage imparted on node 125 is of variable amplitude (“pre-charged to within the supply voltage minus VT” (see col. 4, l. 31)) and hence carries information, both on the exact value or point within the voltage range and on the state of MOSFET channel 100, such as the resistance of the channel, its impurities, etc.., which qualifies it as a signal line according to appellant’s admission.

10.3: Appellant’s third Argument (p. 5, l. 18+):

Appellant’s third argument is that the MOS capacitor is a three terminal device and not a two-terminal device.

Examiner disagrees for the following reason: source and drain are short-circuited and hence form one terminal, and hence the number of terminals =2, and hence in no way different from the number of terminals in a gated diode.

10.4: Appellant's fourth argument (p. 5, l. 26+):

Appellant's fourth argument alleges that "[T]he examiner, however, also equates the gate of alleged isolation device 110 with the control terminal cited in claim 24", thus the "the control signal is essentially the same as the signal to be amplified", from which appellant concludes that "Folmsbee does not disclose or suggest determining that a voltage on a signal line is to be amplified and does not disclose or suggest wherein the control line is coupled to a second terminal of a two terminal semiconductor device, as required by claim 24".

Examiner disagrees for the following reason: appellant is incorrect, because the "control signal" is strictly separate from the control terminal of the isolation device: instead, clock signal ϕ' was identified as the 'control signal'. See page 3, line 12, of the appealed Final office action, which is to be distinguished from the 'control terminal' of the isolation device, 'control terminal' being synonymous in the active solid-state device art with 'gate'. Appellant's lack of clarity as to how the configuration of Folmsbee could function as an amplifier is thus clearly seen to be due to an interpretational error.

10.5: Appellant's fifth argument, in appeal of the rejection of claim 25 (p. 6, l. 9+):

Appellant's argument is that "no addition of voltages can take place" because "the voltage at the gate of NMOS transistor 110 ***is*** the voltage at node 125", while, "contrary to the Examiner assertion, the gate is not in series with said node 125".

Examiner disagrees for the following reason: the claim describes a method, in which a voltage is imparted on a line. It is in this context that the dependent claim was interpreted. The arrival of a signal at node 125 certainly adds to the gate voltage of the isolation device because there is a direct connection from node 125 to said gate. Whether said direct connection is in series or not the addition of an initial voltage at the gate by the arriving signal is met. It is fully in line with normal nomenclature in the electrical arts to characterize a node and a directly connected gate as being "in series". The supposition by appellant that the voltage at node 12 5 and at the gate of 110 are exactly the same neglects line resistance, inductance and capacitance and hence its applicability depends on signal time scales and particulars of the node-gate connection as well as the properties of the gate itself, as known in the electrical arts by those of ordinary skill.

For all of the above reasons, examiner believes the rejections are to be affirmed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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